REMARKS

I. Formal Matters.

Claims 3, 5 and 7-10 are all the claims pending in the application. Claims 1, 2, 4, 6 and 11 were previously cancelled. Applicant thanks the Examiner for withdrawing the finality of the Office Action dated May 3, 2005. Applicant also appreciates the Examiner's withdrawal of the prior rejection of claim 3 under 35 U.S.C. §102.

II. 35 U.S.C. §103(a).

The Examiner rejects claims 3 and 10 as being unpatentable over *Meszko* (U.S. Patent No. 6,327,299) in view of newly cited *Igarashi, et al.* (U.S. Patent No. 6,466,632 B1) (*"Igarashi"*) under 35 U.S.C. §103(a).

Claim 3. The Examiner acknowledges that "*Meszko* fails to disclose that the delay amount control circuit calculates an average amplitude of the comparison signal output from said comparator, and controls said delay circuits so that the average amplitude is equal to or lower than a threshold value, whereby the difference in delay times between said two transmission units is converged to a permissible and acceptable value range" (OA page 3). The Examiner asserts that "the use of an average circuit, usually a low pass filter, and a threshold comparator are very well known." (OA page 3) However, the Examiner does not assert that an averaging circuit and comparator, as utilized in the subject claim, are well known. Therein, the Examiner relies on *Igarashi* to teach the claim subject matter acknowledged to be lacking in *Meszko*. The Examiner asserts that *Igarashi* teaches a delay amount control circuit, calculates an average amplitude of a comparison signal and controls the delay circuits so that the average is below a

given threshold (OA page 3). More specifically, the Examiner cites to *Igarashi* at Fig. 16 and col. 15, line 40 to col. 16, line 29 (OA page 3).

Turning to *Igarashi* at col. 15 lines 40-45, we find that *Igarashi* discloses an averaging circuit 74 and a comparison circuit 75 in Fig. 16. Further, *Igarashi* teaches that adder 73 adds *received* signal powers 701 and 702 to obtain a sum of received signal powers 703. Averaging circuit 74 averages the sums (703) for a period of time to obtain an average sum *received* signal power, which is then compared to a threshold value (*Igarashi* col. 15, lines 56-62).

In contrast, claim 3 requires, comparing detected [transmission] signals and generating a comparative signal. And then, calculating an average amplitude of comparison signals output from the comparator. *Meszko* fails to teach comparing detected signals, generating a comparative signal, and calculating an average amplitude of comparison signals (OA page 3). Secondary reference *Igarashi* fails to provide this deficiency (*Igarashi* col. 15, lines 56-62).

Igarashi teaches summing received signal powers and averaging sums, and then comparing the averaged signal to a threshold, therein *determining the selection of either a diversity reception circuit, or the output of a least squares combining circuit* (col. 15 line 50 -col. 16, line 7). In contrast, claim 3 requires, "*controlling the delay circuits* on the basis of the comparison signal so that modulation timing of RF signals to be transmitted from said two transmission units are coincident to each other". *Meszko* fails to provide controlling delay circuits on the basis of the comparison signal (OA page 3). Secondary reference, *Igarashi* fails to provide this deficiency; where *Igarashi* teaches averaging summed received signals *to select* a best signal quality from the available outputs. *Meszko* and *Igarashi*, either alone or in combination, fail to teach or suggest each and every element required by claim 3. At least for this deficiency, the

rejection of claim 3 as being unpatentable over *Meszko* in view of *Igarashi* under 35 U.S.C. §103(a) should be withdrawn.

The rejection of claim 3 as being unpatentable over *Meszko* in view of *Igarashi* under 35 U.S.C. §103(a) fails on second grounds. The Examiner asserts that the motivation to employ the teachings of *Igarashi* into the transmitter of *Meszko* is to avoid fast variation due to noise. Adding the signals output by the transmitters (or adding detection signals) is not going to reduce the noise of future output signals and is not going to avoid fast variation caused by noise. *Igarashi* teaches a diversity receiver resilient to co-channel interference and fast fading (abstract; col. 3, lines 62-67). Applicant claims a transmitter with modulation timing to provide coincident outputs (*Application* abstract). There is no motivation to employ noise compensation teachings (*Igarashi*) in control of delay units to obtain coincident emissions, required by claim 3. The Examiner's asserted motivation to combine the summing, averaging, and comparing taught by *Igarashi* with the transmitter taught by *Meszko* fails. At least for failing to provide a motivation to combine, the alleged unpatentability of claim 3 *Meszko* in view of *Igarashi* under 35 U.S.C. §103(a) should be withdrawn.

Claim 10 is asserted as being allowable at least by virtue of its dependence upon an allowable claim.

The Examiner rejects claim 5 as being unpatentable over *Meszko* in view of newly cited *Ikegami, et al.* (U.S. Patent No. 4,849,990 A) under 35 U.S.C. §103(a).

Claim 5. The Examiner acknowledges that *Meszko* fails to teach or suggest that "the delay circuit is provided at the input side of the modulator, and therein relies on *Ikegami* to

provide this subject matter. The Examiner cites specifically to *Ikegami* at Fig. 1, block 11 and col. 5, lines 57-62 (OA page 5).

Turning to *Ikegami*, we find that *Ikagami* teaches dividing a signal received at a transmitter into two signals. Sending one signal directly through a modulator and the second signal through a delay circuit and then through a second modulator. The mobile stations, then receive the two signals having a delay time difference provided by the one delay circuit (*Ikagami* abstract, Figs. 1 and 2, element 112 and 112'; col. 1, lines 32-37; col. 5, lines 57-64).

In contrast, claim 5 requires, " . . . each of said plural transmission units further comprises a modulator, a frequency converter and an amplifier, and said delay circuit is provided at the input side of said modulator; and wherein a delay circuit is provided at the input of each modulator. *Ikagami* fails to teach or suggest a delay circuit at the input of each modulator. Further, *Ikagami* teaches away from the requirements of claim 5 by transmitting a pair of signals, where one signal of each pair passes through a delay circuit and is then modulated, and the second signal passes directly through a second modulator.

Meszko fails to provide a delay circuit at the input of each modulator, and *Ikagami* fails to provide this deficiency. At least for failing to teach or suggest, alone or in combination, a delay circuit preceding each modulator, the rejection of claim 5 as being unpatentable over *Meszko* in view of *Ikagami* under 35 U.S.C. §103(a) should be withdrawn.

The Examiner rejects claims 7 and 8 as being unpatentable over *Meszko* under 35 U.S.C. §103(a).

Claim 7. The Examiner asserts that the single block enclosing a filter, an upconverter, and an amplifier *behind* the delay block demonstrates that the position of the delay block relative

to a frequency converter or relative to an amplifier is patentably insignificant (*Meszko*, Fig. 1). Therefore, the Examiner asserts the required claim subject matter of " . . . said delay circuit is provided between said frequency converter and said amplifier . . ." is obvious in view of *Meszko* (claim 7; OA page 6).

Clearly *Meszko* fails to teach or disclose a delay unit between a frequency converter and an amplifier. Is a delay circuit between a frequency converter and an amplifier obvious? Turning to case law, we find that the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice(*In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975); MPEP §2144.04(VI)(C)).

However, "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims [being rejected] is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." (*Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984; MPEP §2144.04(VI)(C)). And therein the Examiner fails to make a prima facie case of obviousness. *Meszko*'s Fig. 1 may suggest that the order of the filter, the upconverter, and the amplifier are interchangeable, however, the delay circuit is clearly shown and described as preceding all three (col. 3 line 41- col. 4 line 4). *Meszko* fails to suggest either in Figures or in the text that a delay circuit is provided between said frequency converter and said amplifier. At least for this deficiency, the rejection of claim 7 as being obvious over *Meszko* under 35 U.S.C. §103(a) should be withdrawn.

Claim 8. The Examiner makes an analogous assertion of obviousness in rejecting claim 8 as discussed above in the traversal of the rejection of claim 7 (OA page 7). The Examiner asserts that the required claim subject matter of " . . . said delay circuit is provided at the output side of said amplifier . . ." is obvious in view of *Meszko* (claim 8; OA page 7; *Meszko* Fig. 1). As demonstrated above, *Meszko* shows in Fig. 1 and describes in the associated text that the delay circuit precedes the combination of a filter, an upconverter, and an amplifier. While the arrangement of the elements of the combination is not specified, the placement of the delay circuit as preceding the combination is clearly disclosed and taught (*Meszko* Fig. 1 col. 3 lines 40- col. 4, line 4). *Meszko* fails to teach or suggest a delay circuit on the output side of the amplifier. In fact, *Meszko* arguably teaches away from the subject matter of claim 8 by teaching and disclosing a delay circuit on the input side of the amplifier.

The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." (*Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984; MPEP §2144.04(VI)(C)). Therein the Examiner fails to make a prima facie case of obviousness. *Meszko* fails to suggest either in Figures or in the text that a delay circuit is provided on the output side of said amplifier. At least for this deficiency, the rejection of claim 8 as being obvious over *Meszko* under 35 U.S.C. §103(a) should be withdrawn.

III. Allowable Subject Matter.

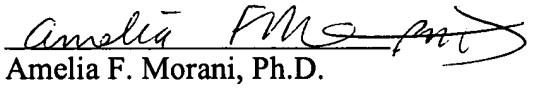
Applicant thanks the Examiner for indicating that claim 9 is allowable.

In view of the preceding amendments and remarks, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points

remain in issue that the Examiner feels may be best resolved through a personal or telephonic interview, he is kindly requested to contact the undersigned at the local telephone number listed below.

The USPTO is directed and authorized to charge all required fees (except the Issue/Publication Fees) to our Deposit Account No. 19-4880. Please also credit any over-payments to said Deposit Account.

Respectfully submitted,



Amelia F. Morani, Ph.D.
Registration No. 52,049

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

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